Attorney's Docket No.: 07977/192001/US3444

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested. The foregoing amendments are responsive to the December 21, 2001 Office Action. Applicants respectfully request entry of the requested amendments and reconsideration of the application in view of the following comments.

Response to objections to the Claims

Claims 81, 83, 85, and 97-101 are objected to as having informalities/defects. The rejection states that the claims recite the term of "said interconnection" but it is indefinite as to which of the two interconnections the term refers. The claims are amended herein to correct any indefiniteness.

Response to the Claim Rejections Under 35 U.S.C § 103

Claims 61, 62, 73-76, and 79-101 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art (AAPA) in view of U.S. Patent No. 4,890,141 issued to Tang, et al or in view of U.S. Patent No. 5,187,122 issued to Bonis. The rejection asserts that the AAPA allegedly teaches each element of the claims except for having a layer comprising metal provided on the insulating surface and directly contacting with

the interconnection, which is allegedly taught by either Tang or Bonis.

The claims are directed toward a device that comprises a thin film transistor and a first interconnection formed over an insulating surface and a layer comprising metal being in direct contact with a first interconnection and being connected with source or drain region of the thin film transistor. The device further comprises a second interconnection connected to the layer comprising metal through a contact hole, wherein the contact hole is located outside the source region, the drain region, and the first interconnection. Figures 1A-1F are annotated and attached to help explain the present invention. Using the present invention, it is not necessary to provide a contact hole on the source, drain regions or the first interconnection. Thus, the size of the thin film transistor and the size of the first interconnection are smaller than that of Figures 2A-2F.

None of the cited art teaches or suggests a device according to the present claims. AAPA teaches that the top layer interconnections 34 and 35 are provided on the source or drain regions and the gate interconnect 25 through a contact hole. Further, Tang teaches that the gate interconnection 212 is connected to the source/drain region 204 through the TiN layer 202. Also, Bonis teaches that the drain 61 is connected

the source 49 through local interconnection 60g. However, neither the AAPA, Tang, nor Boris teach that the contact hole is located outside the source region, the drain region, and the first interconnection, and the effect of the present invention is that the size of the first interconnection is smaller than that of Figures 2A-2F.

In view of the foregoing distinctions, Applicants respectfully submit that independent Claims 61, 73-76, and 86-87 are patentably distinguished over the cited art. Applicants respectfully submit that Claims 61, 73-76, and 86-87 are in condition for allowance, and Applicants respectfully request allowance of Claims 61, 73-76, and 86-87.

Claims 83, 85, and 88-101 depend either directly or indirectly from one of the independent claims. Each dependent claim further defines the independent claim from which it depends. In view of the foregoing remarks regarding Claims 61, 73-76, and 86-87, Applicants respectfully submit that Claims 83, 85, and 88-101 are likewise in condition for allowance. Applicants respectfully request allowance of dependent Claims 83, 85, and 88-101.

Attorney's Docket No.: 07977/192001/US3444

Summary

In view of the above amendments and remarks, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 5/21/02

JAMES T. HAGLER
REG. NO 40,631

Scott C. Harris
Reg. No. 32,030

PTO Customer No. 20985
Fish & Richardson P.C.
4350 La Jolla Village Drive, Suite 500
San Diego, California 92122
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

10185653.doc

Attorney's Docket No.: 07977/192001/US3444

VERSION TO SHOW CHANGES MADE

In the Claims:

Claims 62, 79-82, and 84 have been canceled.

The claims have been amended as follows.

61. (Amended) A display device comprising:

a semiconductor island comprising silicon provided on an insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

[an] a first interconnection formed on said insulating surface;

a layer comprising metal provided on said insulating surface and being in direct contact with said first interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a [top layer] second interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole,

wherein said contact hole is located outside said source region, said drain region and said first interconnection.

73. (Amended) A semiconductor device comprising:

a semiconductor island comprising silicon provided on an insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

[an] a first interconnection formed on said insulating surface;

a layer comprising metal provided on said insulating surface and being in direct contact with said first interconnection and being connected with one of said source region and said drain region, said layer comprising metal being connected with said first interconnection through no contact hole;

an interlayer dielectric provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a [top layer] second interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole,

wherein said contact hole is located outside said source region, said drain region and said first interconnection.

74. (Amended) A semiconductor device comprising:

a semiconductor island comprising silicon provided on an insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

[an] a first interconnection formed on said insulating surface;

a layer comprising metal provided on said insulating surface and being in direct contact with said first

interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric comprising silicon nitride provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a [top layer] second interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole,

wherein said contact hole is located outside said source region, said drain region and said first interconnection.

75. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

a semiconductor island comprising silicon provided over said insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

[an] a first interconnection formed on said insulating surface;

a layer comprising metal provided on said insulating surface and being in direct contact with said first interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric comprising silicon oxide provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a [top layer] second interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole,

wherein said contact hole is located outside said source region, said drain region and said first interconnection.

76. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

a semiconductor island comprising silicon provided over said insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode comprising a doped polycrystalline silicon provided adjacent to said channel region with a gate insulating film therebetween;

[an] a first interconnection formed on said insulating surface;

a layer comprising metal provided on said insulating surface and being in direct contact with said first interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a [top layer] second interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole,

wherein said contact hole is located outside said source region, said drain region and said first interconnection.

83. (Amended) The device of claim 75 wherein said layer comprising metal is connected with said first interconnection through no contact hole.

85. (Amended) The device of claim 76 wherein said layer comprising metal is connected with said first interconnection through no contact hole.

86. (Amended) A display device comprising:

a substrate having an insulating surface;

a semiconductor island comprising silicon provided over said insulating surface;

a source region and a drain region provided in said semiconductor island, said source region and said drain region comprising a silicide of a metal;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

[an] a first interconnection formed on said insulating surface;

a layer comprising said metal provided on said insulating surface and being in direct contact with said first interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric provided over said gate electrode and said layer comprising said metal;

a contact hole provided over said layer comprising said metal in said interlayer dielectric; and

a [top layer] second interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising said metal through said contact hole,

wherein said contact hole is located outside said source region, said drain region and said first interconnection.

87. (Amended) A semiconductor device comprising:

a semiconductor island comprising silicon provided on an insulating surface;

a source region and a drain region provided in said semiconductor island, said source region and said drain region comprising a silicide of a metal;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

[an] a first interconnection formed on said insulating surface;

a layer comprising said metal provided on said insulating surface and being in direct contact with said first interconnection and being connected with one of said source region and said drain region, said layer comprising said metal

being connected with said interconnection through no contact hole;

an interlayer dielectric provided over said gate electrode and said layer comprising said metal;

a contact hole provided over said layer comprising said metal in said interlayer dielectric; and

a [top layer] second interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising said metal through said contact hole,

wherein said contact hole is located outside said source region, said drain region and said first interconnection.

95. (Amended) A display device according to claim 61, wherein said first interconnection is provided in a same layer as said gate electrode.

96. (Amended) A semiconductor device according to claim 73, wherein said first interconnection is provided in a same layer as said gate electrode.

97. (Amended) A semiconductor device according to claim 74, wherein said first interconnection is provided in a same layer as said gate electrode.

98. (Amended) A semiconductor device according to claim 75, wherein said first interconnection is provided in a same layer as said gate electrode.

99. (Amended) A semiconductor device according to claim 76, wherein said first interconnection is provided in a same layer as said gate electrode.

100. (Amended) A display device according to claim 86, wherein said first interconnection is provided in a same layer as said gate electrode.

101. (Amended) A semiconductor device according to claim 87, wherein said first interconnection is provided in a same layer as said gate electrode.